A method for passing a voltage between an internal node inside a memory device and an external pin outside the memory device. The method includes passing an internal voltage from the internal node to the external pin during a read mode. The method also includes passing an external voltage from the external pin to the internal node during a force mode.

IN THE SPECIFICATION

Please make the paragraph substitutions indicated in the appendix entitled Clean Version of Amended Specification Paragraphs. The specific changes incorporated in the substitute paragraphs are shown in the following marked-up versions of the original paragraphs:

The paragraph beginning on page 4, line 29 is amended as follows:

Pass control circuit 120 produces control signals to activate [read] pass circuit 118 to pass a voltage to output pin 116. Pass control circuit 120 comprises first and second n-channel MOS transistors 136 and 138, p-channel transistor 140, and inverter 142. Inverter 142 is coupled between an input signal, [labelled] labeled READ, from a test signal generator on integrated circuit 12 and node 132. The READ signal is also provided to [read] pass circuit 118 at the gate of transistor 124. A gate of transistor 140 and a gate of transistor 138 are coupled to node 132. A source and substrate of transistor 140 are coupled to the supply voltage, V_{cc}. A drain of transistor 140, a drain of transistor 138 and a gate of transistor 136 are coupled together at node 134. A source of transistor 136 is coupled to node 126. Finally, a source of transistor 138 is coupled to a drain of transistor 136 at node 114. Node 114 also receives the voltage to be read by circuit 110.

The paragraph beginning on page 7, line 23 is amended as follows:

At time t_3, pin 216 is isolated from circuit 210. The READ and RESET signals are both taken to ground potential. Node 233 returns to a high logic level and the output of pass control circuit 220 ceases to oscillate at node 230. Further, node 244 stays at ground potential and transistor 242 stays off. Node 254 goes to a high logic level turning on transistor 250 and bringing node 226 to a low logic level so as to turn off transistor 224 and isolate circuit 210 from pin 216. Once isolated, [node 116] pin 216 is allowed to float and decays over time as shown in Figure 5J.